**KEY PRODUCT BENEFITS**
Essential for the most advanced process nodes

- Meets foundries’ required accuracy
- Delivers maximum per-CPU speed & capacity
- Predictable runtime, proportional to the number of transistors
- Scalable capacity over single & multi-CPU
- No need to “design around” the DRC tool to meet hierarchy considerations

**KEY PRODUCT FEATURES**

- One-Shot Window Scan™
- Multi-CPU architecture
- Easy-to-learn powerful rule language
- Easy-to-use GUI

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**Overview**

PowerDRC was architected to address physical verification challenges for today’s deep sub-wavelength nanometer process nodes—40nm and above. PowerDRC is driven by a unique One-Shot Window scanning that allows scalable physical verification applied at the most appropriate level of granularity producing fast, predictable and accurate results across a variety of layout styles. The benefits of One-Shot processing extends perfectly into multi-CPU configuration, delivering performance and capacity that far exceed other DRC tools. In addition, the extra level of IP protection that comes naturally with flat DRC is a unique benefit of the product architecture.

One-Shot Window Scan is a proprietary capability enabling an architectural quantum leap in DRC technology. This One-Shot Window Scan is the foundation of PowerDRC. It enables PowerDRC to be the fastest and highest capacity, flat, full chip DRC solution. The One-Shot Window Scan technology is designed to simultaneously operate on multiple rules/layers and operations (Fig 1). Unlike the traditional DRC tools, one-shot processing runtimes are predictable and proportional to the number of polygons to be processed. With shrinking geometries, the number of transistors and hence the number of polygons per chip increase. With PowerDRC, the runtimes continue to be predictable (Figure 2).

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**Figure 1. One-Shot Processing & Windowing**

**Figure 2. Linear & predictable runtimes**
Multi-CPU Architecture

One-Shot Window Scan delivers the most powerful single-CPU DRC solution, and lends itself well for distributed processing over multiple CPUs without explosion of data. This improves DRC turnaround time and enables large designs to be processed efficiently and effectively. Furthermore, the multi-CPU architecture leverages the predictability of One-Shot blocks to maximize CPU efficiency per rule check.

PWRL design rule language

The rule language of PowerDRC/LVS fits in with current rule deck architectures and flows allowing easy migration from existing PV systems, it also offers the ability to efficiently and effectively model the most complex rules and checks. The syntax allows for performing some of the more complex DRC checks with fewer lines of code resulting in most comprehensive rule decks in terms of coverage with no fear of over- or under-checking.

XOR and QuickDiff capabilities

An XOR run is a special separately licensed mode of DRC that reads two input graphic databases (either or both in GDSII or OASIS, OA and CDBA when run with Cadence Virtuoso) and compares corresponding layers in pairs according to rule file. QuickDiff is a quick check for changes by means of special heuristic algorithms. It is intended primarily to detect differences (or ensure their absence) in two revisions of a given layout close to tapeout. QuickDiff may be used as pre-processing stage for XOR resulting in dramatic speedup of XOR operation.

Fill layers generation with PowerDRC may be done either with rectangles, which size is specified by fill command parameters, at certain distance with or without offsets, either inside or outside the layer. Filling also may be done with a cell that contains arbitrary shapes in several different layers. The developer may attach these layers later as a separate group to some cell/top cell (hierarchically) using a layout editor.